CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A method of fabricating an interconnect structure comprising the steps of:

forming a dense etch stop layer on a surface of a substrate, said dense etch stop layer is capable of protecting underlying metallurgy during a subsequent etching step;

forming a controlled pore glass (CPG) interlayer dielectric on the dense etch stop layer;

subjecting the CPG interlayer dielectric to thermal treatment which allows for spinodal decomposition of the CPG into a distinct interpenetrating microstructure which includes a substantially pure silicon dioxide network and a boron-rich network;

selectively removing the boron-rich network by acid etching to provide a reticulated porous network of substantially pure, amorphous silicon dioxide; and

forming metal wiring within said reticulated porous network of substantially pure, amorphous silicon dioxide.

2. The method of Claim 1 wherein said CPG interlayer dielectric is a material having the formula $R_yO{\cdot}B_2O_3{\cdot}SiO_2$ wherein R is an alkaline earth, alkaline metal or a heavy metal oxide and y is 1 or 2 depending on the valence of R.

3. The method of Claim 1 wherein said thermal treatment is performed in an inert gas ambient at a temperature that is greater than or equal to 350°C

4. The method of Claim 3 wherein said thermal treatment is performed at a temperature from about 400°C to about 600°C.

5. The method of Claim 1 wherein said acid etching comprises use of an inorganic acid selected from the group consisting of hydrochloric acid, nitric acid, nitrous acid, sulfuric acid and water.

6. The method of Claim 1 wherein said reticulated porous network of substantially pure, amorphous silicon dioxide is treated with a hydrophobic agent prior to forming said metal wiring.

7. The method of Claim 6 wherein said hydrophobic agent is a silylating agent.

8. The method of Claim 1 wherein said forming the metal wiring comprises patterning said reticulated porous network of substantially pure, amorphous silicon dioxide to provide at least one opening therein; filling the at least one opening with a conductive metal; and planarizing.

9. The method of Claim 8 wherein said forming the metal wiring further comprises forming a refractory liner in said at least opening prior to filling with said conductive metal.

10. The method of Claim 9 wherein said forming the metal wiring further comprises sealing pores in the at least one opening with a sealant layer prior to forming said refractory metal.

11. The method of Claim 1 further comprising forming a capping layer atop said reticulated porous network of substantially pure, amorphous silicon dioxide and said metal wiring.

12. An interconnect structure comprising:

a substrate having a dense etch stop layer located on a surface thereof;
a patterned interlayer dielectric of a reticulated porous network of substantially pure, amorphous silicon dioxide located on the dense etch stop layer; and

a metal conductive region formed within said patterned interlayer dielectric.

13. The interconnect structure of Claim 12 wherein the dense etch stop layer is a dielectric material that prevents acid from attacking underlying metallurgy present in the substrate.

14. The interconnect structure of Claim 13 wherein said dense etch layer comprises silicon dioxide, silicon nitride, silicon oxynitride, hydrogenated silicon carbide, hydrogenated silicon oxycarbide, or hydrogenated silicon carbon nitride.

15. The interconnect structure of Claim 12 wherein said patterned interlayer dielectric is a controlled pore glass material having a dielectric constant of less than 4.0.

16. The interconnect structure of Claim 15 wherein said controlled pore glass material has a pore size from about 5 to about 15 nm at a volume percent porosity from about 30 to about 70%.

17. The interconnect structure of Claim 12 wherein patterned interlayer dielectric has a surface that is hydrophobic.

18. The interconnect structure of Claim 12 wherein said metal conductive region includes a conductive metal selected from the group consisting of Al, Cu, W, Ag and alloys thereof.

19. The interconnect structure of Claim 18 wherein said conductive metal is Cu.

20. The interconnect structure of Claim 12 wherein said metal conductive region further comprises a refractory liner, sealant layer or combination thereof.